Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method for electrically isolating and analyzing site-specific defects in a MOSFET comprising:
electrically localizing at least one specific site of at least one defective feature of a MOSFET device;
depositing a first cap layer over an exposed metal layer of said MOSFET device to cover said at least one defective feature;
forming at least one opening in said first cap layer over said at least one specific site of said at least one defective feature;
providing said at least one opening with at least one electrical connection;
depositing a second cap layer over a portion of said first cap layer, said second cap layer covering said at least one defective feature and a portion of said electrical connection;
removing said first and second cap layers at least within said at least one specific site of said at least one defective feature to obtain a site-specific junction for imaging;
forming a conductive coating over said site-specific junction; and
analyzing said at least one defective feature within said

site-specific junction via imaging.

[c2] The method of claim 1 wherein the step of providing said MOSFET device with said at least one electrical connection further comprises:
depositing a conductive liner on sidewalls of said at least one opening;
depositing a conductive pad over said first cap layer;
providing a plurality of conductive wiring connections between said conductive liner and said conductive pad; and
depositing said second cap layer over said first cap layer, wherein said second cap layer fills empty portions of said plurality of openings and covers both said at least one defective feature and portions of said conductive wiring connections while leaving said conductive pad region exposed.

[c3] The method of claim 1 further including, prior to the step of removing said first and second cap layers, the step of sequentially polishing a first surface and a second surface of said MOSFET device to within 20 microns of said site-specific junction for imaging.

[c4] The method of claim 1 wherein said first and second cap layers are removed by FIB gallium ion milling.

[c5] The method of claim 4 further including, subsequent to said step of FIB gallium ion milling said first and second cap layers, incrementally milling, in sequence, each of a first surface and a second surface of said MOSFET device to remove implanted gallium ions during said FIB gallium ion milling, as well as remove any damaged layers of said MOSFET device.

[c6] The method of claim 1 wherein said MOSFET device comprises a sub-micron MOSFET device having source/drain junctions less than about 80 nm deep with junction lengths less than about 100 nm.

[c7] The method of claim 1 wherein said MOSFET device further includes a substrate layer comprising a material selected from the group consisting of bulk silicon, silicon on insulator, strained silicon junctions and combinations thereof.

[c8] The method of claim 1 wherein said metal layer comprises a material selected from the group consisting of tungsten, tungsten carbonyl, platinum, nickel, alloys thereof and combinations thereof.

[c9] The method of claim 1 wherein said conductive coating comprises a conductive carbon coating deposited to a thickness ranging from about 75 angstroms to about

150 angstroms.

[c10] The method of claim 1 wherein said at least one defective feature within said site-specific junction is analyzed via holographic imaging.

[c11] The method of claim 10 wherein said at least one defective feature is selected from the group consisting of blocked implants, asymmetric doping, channel length variations and combinations thereof.

[c12] A method for electrically isolating and analyzing site-specific defects in a MOSFET comprising:
electrically localizing at least one specific site of at least one defective feature of a MOSFET device;
exposing a metal layer of said MOSFET device residing over said at least one defective feature;
depositing a high-k cap layer over said exposed metal layer to cover said at least one defective feature;
forming at least one opening in said high-k cap layer over said at least one specific site of said at least one defective feature, said at least one opening stopping at a top surface of a metallization layer in contact with said defective feature of said MOSFET device;
coating sidewalls of said at least one opening with a conductive liner;
providing at least one electrical interconnection within

said at least one opening in a direction leading away from the underlying MOSFET device;
depositing a metal cap layer over a portion of said high-k cap layer to fill empty portions of said at least one opening so as to contact said metallization layer within said opening, said metal cap layer covering said at least one defective feature and a portion of said electrical interconnection;
collimated ion milling said high-k and metal cap layers at least within said at least one specific site of said at least one defective feature using a low energy noble gas to obtain a site-specific junction for holographic imaging;
forming a conductive coating over said site-specific junction; and
analyzing said defective feature within said site-specific junction via high resolution electron holographic imaging.

[c13] The method of claim 12 wherein the step of exposing said metal layer of said MOSFET device comprises removing at least one layer over said MOSFET device in a noble gas atmosphere using an ion beam having an energy of less than about 600 electron volts and at an angle ranging from about 12 degrees to about 20 degrees, therein avoiding damage to a low-k dielectric layer of

said MOSFET device.

[c14] The method of claim 12 wherein said high-k cap layer is deposited to a thickness ranging from about 600 angstroms to about 1500 angstroms.

[c15] The method of claim 12 wherein said high-k cap layer comprises a material selected from the group consisting of tetraorthosilicate, diethyl silane, titanium isoproproxide, RF deposited oxide, RF deposited nitride and combinations thereof.

[c16] The method of claim 12 wherein said conductive liner comprises a material selected from the group consisting of tungsten, tungsten carbonyl, platinum, nickel, alloys thereof and combinations thereof, deposited to a thickness ranging from about 50 angstroms to about 300 angstroms.

[c17] The method of claim 12 wherein the step of providing said at least one electrical interconnection within said at least one opening in the direction leading away from the underlying MOSFET device comprises depositing a conductive probe pad region on said high-k cap layer at a distance ranging from about 10 microns to about 20 microns away from said at least one defective feature, and said electrical interconnection is provided between said

conductive liner within said opening and said conductive probe pad region.

[c18] The method of claim 12 further including, before the step of forming said conductive coating over said site-specific junction, incrementally milling, in sequence, each of a first surface and a second surface of said MOSFET device to remove any implanted milling ions and remove any damaged layers of said MOSFET device, as well as provide said site-specific junction with a thickness ranging from about 200 nm to about 350 nm for said holographic imaging step.

[c19] The method of claim 12 wherein said MOSFET device is affixed to a carbon planchet on a cooled rotating stage of an ion beam milling tool to obtain planar surface areas of said MOSFET device during said processing steps as well as form said conductive coating over said site-specific junction comprising a conductive carbon coating.

[c20] A method for electrically isolating and analyzing site-specific defects in a MOSFET comprising:
electrically localizing a specific site of a defective feature of a MOSFET device;
depositing a high-k cap layer over an exposed metal layer of said MOSFET device to cover said defective fea-

ture;
forming an opening in said high-k cap layer over said specific site of said defective feature;
depositing a conductive liner on sidewalls of said opening;
depositing a conductive pad region over a portion of said high-k cap layer;
providing at least one conductive wiring connection between said conductive liner and said conductive pad;
depositing a metal cap layer over said high-k cap layer, said metal cap layer filling empty portions of said opening and covering both said defective feature and portions of said conductive wiring connection while leaving said conductive pad region exposed;
sequentially polishing a first surface and a second surface of said MOSFET device to within 20 microns of said specific site of said defective feature
trimming said high-k and metal cap layers within said polished regions of said MOSFET device via FIB ion milling to obtain a site-specific junction for holographic imaging;
incrementally milling, in sequence, each of said first and second surfaces to remove any implanted milling ions as well as remove any damaged layers of said MOSFET device, said incremental milling step providing said site-specific junction with a thickness ranging from about

200 nm to about 350 nm;

forming a conductive coating over said site-specific junction; and

analyzing said defective feature within said site-specific junction via high resolution electron holographic imaging in a transmission electron microscope.